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# Al thermomigration applied to the formation of deep junctions for power device insulation

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**Abstract**

An alternative method for creating total vertical junction insulation of power devices is presented. It involves the thermomigration of melted Al/Si. The method is first theoretically presented together with the specifically designed rapid thermal processor used in the experiments. Physical and electrical results are then given showing the efficiency of the method in terms of thermal budget, surface consumption and voltage handling capability. The issue of manufacturability is finally addressed. 

## 1. Introduction

Applications requiring high voltage levels imply a vertical design of the power component. In addition, applications such as circuit breakers for protection require the fabrication of two-direction structures associating, in the same chip, different building blocks [1]. These architectures occupy the whole silicon thickness and emerge on both sides [2]. Highly doped vertical walls are therefore required both for total vertical junction insulation of devices, and alternatively as a permanent conducting link between device surfaces.

The generally used method of fabrication for these junctions extending through the thickness of the wafer is based on a high (1300°C) temperature redistribution during several days (300 h) applied to relatively thin (200 $\mu$m) wafers. The obtained junctions are about twice as wide as their depth, leading to a large surface consumption. Moreover, the wafer warpage after redistribution jeopardizes the following process steps, and the induced surface defects are incompatible with the fabrication of MOS gates [2].

We have investigated an alternative method called temperature gradient zone melting (TGZM) for creating these doped walls. It involves the thermomigration of melted Al/Si. The basic advantages of the method are in terms of thermal budget and surface consumption. The method is briefly presented below.

## 2. Theory of thermomigration

During TGZM, a molten Si/Al solution moves through a single-crystal Si wafer in minutes, leaving a highly Al doped trail behind it. This liquid phase diffusion is driven by a vertical thermal gradient to be created in the wafer.

In our experiments, this gradient is created by a properly designed rapid thermal processor (RTP) which also heats the wafer at a temperature well above the Al/Si eutectic point. The small temperature gradient in the liquid induces a slight Si concentration gradient causing Si liquid diffusion from the hot to the cold interface. This creates undersaturation and oversaturation conditions at the hot and cold interfaces, respectively. New silicon atoms will be supplied by the substrate at the hot interface, while others will be deposited at the cold one. Al diffuses in the opposite direction, and the two effects combine to create the global movement of the liquid solution against the temperature gradient through the wafer.

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Side diffusion is small, and the resulting doped area is single-crystal. As the droplet moves, it leaves behind it a tail of Al heavily doped p-type silicon. The Al concentration is given by the solid solubility of Al in Si at the process temperature. It is worth mentioning that the work presented below is not the first attempt to use rapid thermal processing for creating PN junctions via formation of Al–Si eutectic, see for instance the recent work of Nagel et al. [3], and that TGZM is also being used for micro-sensors fabrication as in Campbell et al. [4].

## 3. Process Description

Aluminum layers are first evaporated on (100) phosphorus-doped, 380 $\mu$m thick wafers. These layers are then etched to create the desired patterns which are built of lines oriented in (011) directions. These directions were demonstrated to be the only line directions giving stable migration in the (100) direction [5]. We chose to work on (100) wafers because the issue of (111) wafers has already been treated successfully in the literature [6], and because (100) orientation is of interest for power devices.

The wafers are heated in the RTP furnace presented below. The design of this furnace provides a vertical thermal gradient through the wafer thickness and allows the liquid Al–Si alloy to migrate towards the hottest side of the wafer. More precisely, the patterned surface of the wafer faces a heat sink. The wafer temperature is first increased and then kept nearly constant (the system is power controlled), allowing the molten Si–Al solution to move through the wafer thickness from the cold (patterned) to the hot (i.e. illuminated) surface. The emergence of the melted alloy is detected optically in situ. After the TGZM step, the wafer is mechanically polished on both sides to remove residual Si–Al alloys.

## 4. Furnace description

Wafers up to 6" in diameter are annealed in a rapid thermal processor specifically designed by AET Technologies. It is made up of a single row of 15 bar-shaped tungsten halogen lamps cooled by forced convection and suspended below a water-cooled reflector, on one side of a processing chamber. A black water-cooled base on the other side acts as a radiative heat sink. The task of this base is critical: it has to absorb the radiation emitted by the non-illuminated surface of the wafer, to create a controlled temperature gradient between the back and front surfaces of the wafer. About 90 kW total power can be applied to the lamps under 400 V mains. Temperature or power cycle is microprocessor controlled. For safety purposes, the temperatures of the water and air used for cooling are monitored at the outputs. Power control is normally used, the 15 lamps being arranged in 7 independent zones. Wafer maximum temperature is 1412°C, that is the Si melting point. Maximum ramp-up rate used is about 50°C/s.

The processing chamber is 20,5 cm in diameter and is isolated by two air-cooled quartz windows, from the lamps on one side, and from the heat sink on the other. The processor is equipped with viewports allowing the visual observation of the wafer's illuminated surface. A video camera and a recorder are available. An optical pyrometer is aimed at the wafer's non-illuminated surface. SiC guard rings eliminate stray light effects on the sensor and prevent unwanted radial gradients from developing in the wafer. For the same purpose, the wafer can be rotated up to 40 rpm. The annealings are performed in nitrogen.

Uniformly illuminating, only the front side of the wafer leads to a temperature gradient perpendicular to the wafer surface. This gradient can be simply estimated assuming that the heat loss from the back side of the wafer is by radiation, with input from the other side and vertical conduction through the wafer thickness. This yields:

$$A\epsilon\sigma T^4 = KA\frac{\Delta T}{t} \tag{1}$$

where $A$ is the wafer area (cm$^2$), $\epsilon$ is the silicon emissivity (dimentionless) $\sigma$ is the Stefan–Boltzmann constant ($5.62.10^{-12}$ W/cm$^2$ K$^4$), $T$ is the temperature of the back side of the wafer (K), $K$ is the Si thermal conductivity (W/cm K), $\Delta T$ is the temperature difference between front and back side, and t is wafer thickness (cm). The thermal gradient within the wafer thickness is therefore given by:

$$\frac{\Delta T}{t} = \frac{\epsilon\sigma T^4}{K}. \tag{2}$$

The gradient is temperature dependant through $T^4$ and $K$. Its maximum value (136 K/cm if $\epsilon = 0.6$ and $K = 0.2$ W/cm K) is obtained at the Si melting point (1685 K). To foster migration speed, a high gradient is needed: this implies that the wafer backside (i.e. non-illuminated side) freely radiates without any incoming radiation either emitted or reflected by the surroundings.

The heat sink therefore needs to be non-reflective and its temperature has to be kept to a sufficiently low level to avoid any thermal emission. The power $P$ to be absorbed can be estimated by assuming that the Si wafer and the SiC guard ring are at the same temperature and exhibit the same emissivity. $P$ is then given by:

$$P = \epsilon\sigma T^4 \frac{\pi d^2}{4} \quad (3)$$

where $P$ is the emitted/absorbed power (W) and $d$ the processing chamber diameter (cm). Considering the numerical values already given, this equation yields:

$$P = 9\ \text{kW}. \quad (4)$$

A temperature below 100°C for the heat sink assures reproducible results for such a chamber arrangement [7], with the added advantage of permitting the use of water for the heat sink cooling. A water flow of 12 l/min was choosen. Given the above value for the absorbed power, it is theoretically enough to limit the increase of the cooling water temperature to 10°C, provided that the water flow is laminar. This is why the heat sink is made of 34 rectangular copper pipes soldered together and coated with light absorbing paint.

The total flows for cooling are about 160 $m^3$/h for air, and 30 l/min for water. During a process, the lamps are linearly ramped over 10–30 s to a given power setting, and held at that value for a few tens of seconds. The duration needed for the melted alloy to migrate through the wafer is experimentally determined by the observation of the wafer illuminated surface. The lamps are shut off when the aluminium pattern appears.

## 5. Experimental results

The physics of the stability of the droplet migration and the corresponding unwanted side-effects have been presented in details in Ref. [8]: solid silicon balls may be left on the entrance surface, the roughness of the entrance surface may be increased, droplets may break-up, and finally there is always an end expansion of the droplet at the exit surface. All these undesired phenomena are related to the process temperature (and therefore the speed of migration) and to the size of the droplet, that is the thickness and width of the lines initially patterned on the entrance surface.

Given the application considered above, that is isolation of power devices, the key issue is the obtention of continuous walls extending through the wafer thickness. We have, therefore, studied various combinations of the above parameters to obtain very few line breaks. Numerous observations revealed that a great majority of line breaks occured at the entrance surface, at the very start of the process.

Aluminum layers (between 1 and 5 $\mu$m in thickness) were evaporated and then patterned to create 4 × 4 mm squares, the wall width of which ranged from 25 to 125 $\mu$m (from square to square). In the following, TGZM duration was about 45 s.

In Fig. 1, a cross section of a wafer after completion of TGZM is exhibited. It shows a highly aluminum-doped region extending through the wafer thickness. It can be noticed that the edges of this $P^+$ region are quite flat and vertical, as a result of a thermal gradient perpendicular to the wafer surface during the annealing ; they are parallel everywhere but near the sample exit surface. This end expansion, described by Chang [8], cannot be avoided but is quite predictable, and can be reduced to the cost of a lower temperature during TGZM (and therefore, a longer duration for

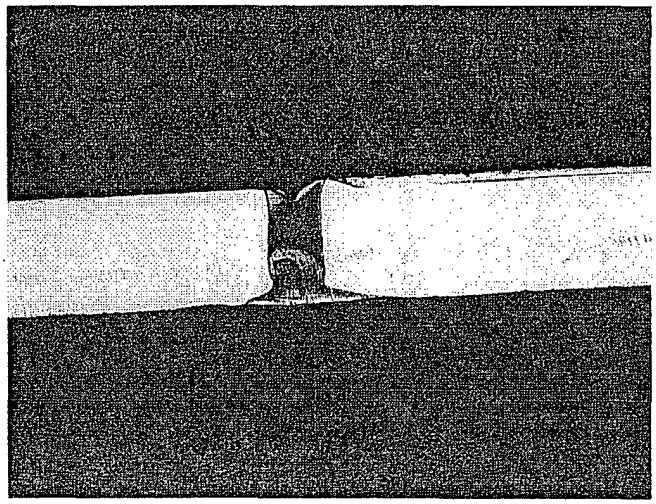

Fig. 1. Cross section of a TGZM junction—the doped recrystallized material is stained to reveal the migration path. Entrance side is up.

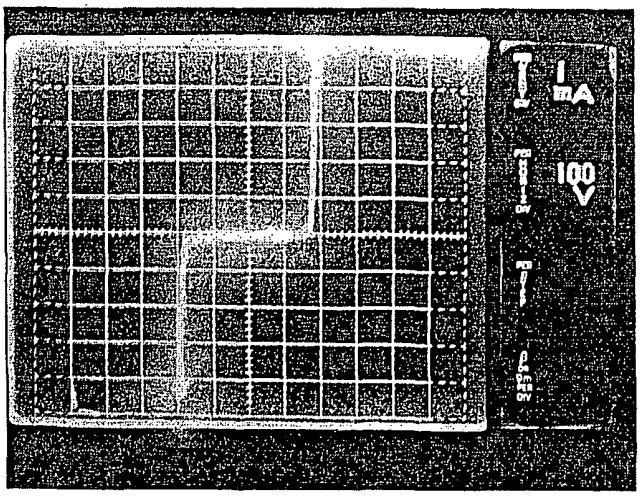


Fig. 2. $I(V)$ characteristic of a $NP^+N$ structure—the electrical contacts are on the N Si substrate on either sides of the $P^+$ wall.

thermomigration). It can be removed by chemical mechanical polishing. With respect to wall break-up, the best choice for Al thickness is 3 $\mu$m. In this case, all walls are continuous whatever their thickness.

According to $I(V)$ electrical measurements (see Fig. 2), the created $P^+N$ junctions exhibit good characteristics: their mean breakdown voltage is 200 V with a donor concentration of $2 \times 10^{14}$ cm$^{-3}$ and a forward voltage of 400 mV. The relatively low breakdown voltage may be considered as caused by the sharp corners of the square paterns which concentrate the electric field. However, with respect to voltage handling, the yield needs to be improved, as some structures exhibited low breakdown voltages.

While these results are encouraging, a question arises: if included in a comprehensive process, what is the best moment for performing TGZM? Is it at the beginning of the process, with the risk of a large Al redistribution resulting from the high temperature steps still to be done, or is it at the end with the danger of damaging the already fabricated structures? This last point is a strong obstacle to TGZM: a positive answer today may not last long in the future as the above structures become more and more sophisticated [2].

While seeking a more definitive preliminary answer, we have submitted a TGZM sample to annealing (1100°C, 12 h) corresponding to a typical thermal budget associated with the fabrication of the two-direction structures mentioned in the introduction [2]. The subsequent Al redistribution was experimentally found to increase the TGZM wall thickness by only 18 $\mu$m on each side as shown in Fig. 3, where the darkest area corresponds to the initially doped region. This result is in good agreement with a process simulation we have also conducted. The TGZM advantage in terms of Si area consumption is therefore maintained vs conventional methods, even if thermomigration is performed at the very beginning of a process.

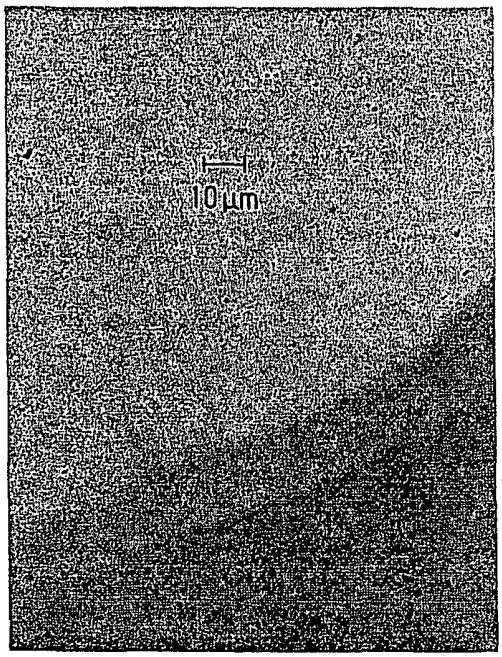


Fig. 3. Cross section of a TGZM junction showing Al redistribution after annealing—the doped recrystallized material is stained as in Fig. 1. The picture is taken in the end expansion area (see text).

## 6. Conclusion

Although further investigations are needed, the experimental results obtained with TGZM are encouraging. TGZM technology is a very attractive tool for the manufacturing of power components. It may open a new dimension for device design.

Future work will include more investigations of manufacturability aspects, that is, the compatibility of the method with a comprehensive process for the fabrication of power integrated circuits. The handling capability issue will also be considered.

It is worth mentioning that RTP is probably today the simplest technology able to achieve TGZM. In addition, the issue of the accuracy of the temperature measurement, which is still a problem in RTP, is not of great importance for the method presented above. Nevertheless, a specific design of the rapid thermal processor is needed, first to operate at high temperature levels, and then to create the required vertical temperature gradient.

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